1C8113

Roll No. _____ Total No. of Pages: 2

1C8113

M.C.A. I-Sem. (Main / Back) Exam., 2026

MCA-104 Computer Architecture

Time: 3 Hours

Maximum Marks: 70
Min. Passing Marks: 28

Instructions to Candidates:

Attempt all Ten questions from Part A. All five questions from Part B and three questions out of five questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (As mentioned in form No. 205)

1. NIL 2. NIL

PART – A

[10×2=20]

(Word limit 25)

Q.1 What is DMA?

Q.2 Define Multi Processing.

Q.3 What are Latches?

Q.4 What is Control Register?

Q.5 What is micro operation?

Q.6 Define Assembler.

Q.7 Define Page Hit Ratio.

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Q.8 What is Sequential Circuit?

Q.9 What are the limitations of D flip-flop?

Q.10 What is Linking?

PART – B

[5×4=20]

(Word limit 100)

Q.1 Explain different types of data transfer modes.

Q.2 Explain the concept of shared memory.

Q.3 Explain Interrupt and Interrupt Cycle.

Q.4 What is Distributed Computing?

Q.5 Describe Cache and Associative Memory.

PART – C

[3×10=30]

(Attempt any three questions)

Q.1 Explain memory organization and memory hierarchy.

Q.2 Draw and explain functional block diagram of 8085 Processor.

Q.3 Describe Vector and Array Processing.

Q.4 Describe Synchronous and Asynchronous Data Transfer.

Q.5 What is hardwired control? Explain.

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